# Large Signal GaAs MESFET Oscillator Design

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*Abstract*—**Techniques for large signal GaAs MESFET oscillator design are described which do not require repeated large signal measurements. In the first technique, small signal *S*-parameter measurements are used with a computer program to compute the packaged and mounted device equivalent circuit. Large signal measurements are made to determine a mathematical relationship between only those parameters which vary under large signal conditions. These relationships are included in the computer program. Then, once the equivalent circuit has been computed from the small signal *S*-parameter measurements, those parameters varying under large signals are incrementally altered until large signal *S* parameters are obtained which correspond to maximum oscillator output power. These values are used to calculate embedding element values for six oscillator topologies. A coaxial cavity FET oscillator was built and tested using the large signal design theory, and it substantially verified the design technique.**

**The second design technique is based on the fact that $S_{21}$ varied more than other *S* parameters under large signals. By making design calculations based on $S_{21}$ reduced to the point corresponding to maximum oscillator power, it was possible to get usable design information for an FET oscillator.**

## I. Introduction

LARGE SIGNAL amplifier and oscillator design has always been a somewhat difficult procedure, generally requiring extensive large signal measurements. Recently, an article by Vehovec, Houselander, and Spence [1] appeared, discussing a method of two-port device oscillator design that maximizes the output power. This method, based on known device *Y* parameters, resulted in linear equations for the embedding elements, with the only assumption being that the voltages are nearly sinusoidal. This requires either or both of the following conditions: 1) that the nonlinearity be of a small degree, or 2) that the embedding network satisfy Aiserman's [2] filter hypothesis. The nonlinearity of a GaAs MESFET is quite small, as evidenced by its large dynamic range and large third-order intercept in an amplifier. Thus the GaAs FET is well suited to the type of analysis used by Vehovec.

More recently, Kotzebue and Parrish [3] extended the work of Vehovec and derived a set of closed form solutions for the embedding elements of three series-type oscillators and three shunt-type oscillators. Kotzebue [4]–[6] developed a technique for large signal *Y*-parameter measurements at microwave frequencies, and successfully used them in large signal amplifier design. The advantage of *Y*-parameter measurements is that they are measured with a short-circuited input or output; hence, there is no uncertainty as to the magnitude of the output voltage, as there is in large signal *S*-parameter measurements.

The difficulty with large signal *Y*-parameter measurements is that it is very difficult to obtain a good RF short circuit at the device terminals, particularly at microwave frequencies. While Kotzebue described a technique for making these measurements, they are not particularly easy, since no large signal measurements, either *S* or *Y* parameter, are particularly "easy" for the amplifier designer who would prefer to use data supplied by the manufacturer. *S*-parameter measurements are more readily accomplished than *Y*, but there is still the uncertainty of the input signal level relative to the output. Furthermore, harmonic effects further render measurements uncertain.

In spite of these limitations, Leighton *et al.* [7] were able to design successfully a large signal amplifier based on large signal *S*-parameter measurements. Maeda *et al.* [8] obtained meaningful oscillator design data at least for the oscillation frequency based on small signal *S*-parameter measurements. Besser [9] also obtained meaningful design information based on small signal measurements. More recently, Mitsui *et al.* [10] developed a MESFET oscillator design method using large signal *S* parameters. They obtained good agreement between measured and predicted performances of an MIC oscillator. Finally, the work of Gonda [11] should be mentioned in which he obtained design data from measurements of a partially built oscillator viewed as a one-port device.

In this paper two alternative approaches to large signal FET oscillator design will be described which do not require repeated large signal device measurements, but which are based upon large signal measurements.

## II. Theoretical Study

### A. Design Approaches

The first approach, which is described in detail in the remainder of this paper, is as follows. For the FET device to be used, small signal *S*-parameter measurements are made at several frequencies (or the data are obtained from the manufacturer). The *S* parameters measured, along with estimated device equivalent circuit values including package parasitic elements, are then inputted to a com-

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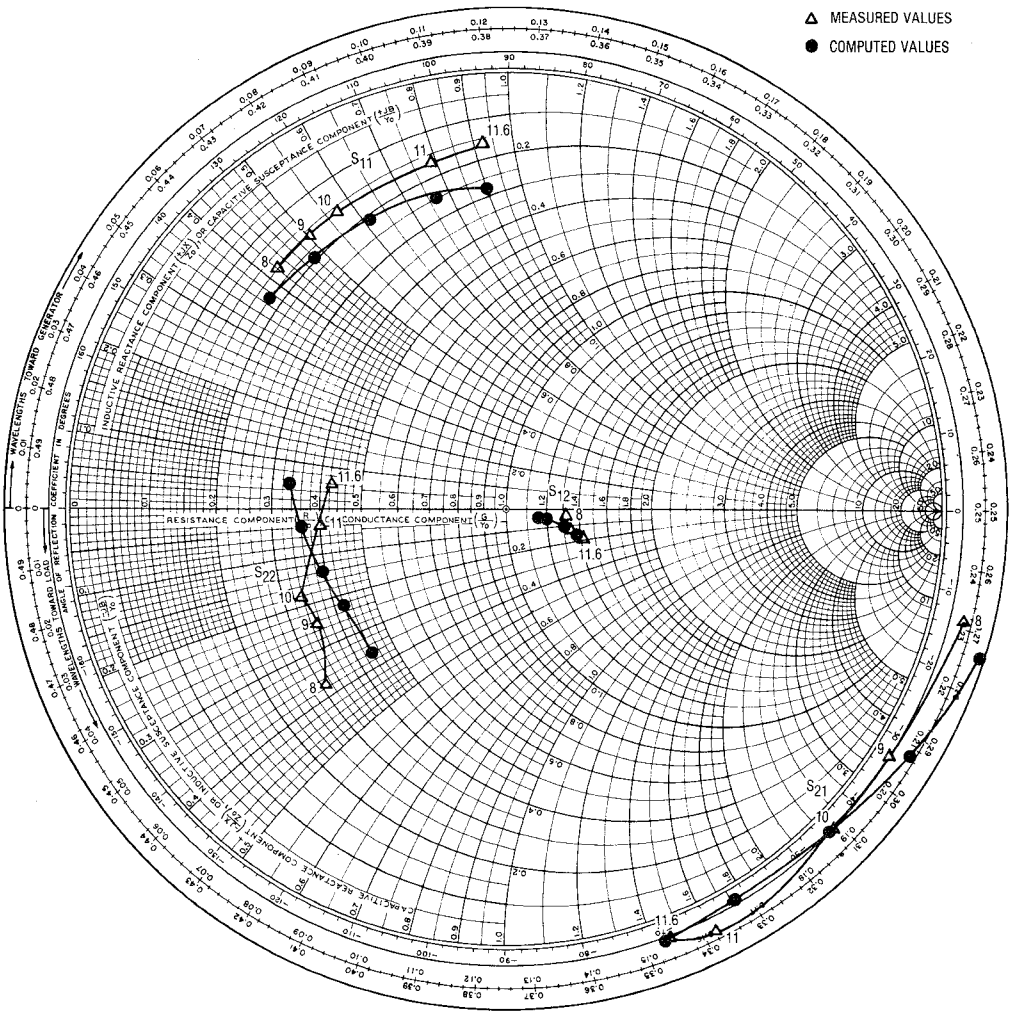



Fig. 1. GaAs FET computed and measured $S$ parameters.

puter optimization program such as the one described by Vendelin and Omori [12]. The computer program is designed to match the measured $S$ parameters to the $S$ parameters computed for the device from its equivalent circuit. The computer output gives the computed $S$ parameters, which match the inputted parameters, plus the equivalent circuit values for the active FET device and the package parasitics.

The next step, carried out by the computer, is to vary in a previously defined manner those elements of the equivalent circuit which vary under large signals. The argument here is that only a few of the equivalent circuit elements vary under large signals. Hence, it should be possible to determine which elements do vary significantly and to develop some mathematical relationship between the variable elements. Once having determined the elements which vary under large signals and their relative changes as the signal level increases, these relationships may be included permanently in the computer program. The computer, after computing the small signal equivalent circuit values, then incrementally alters only those elements which vary under large signals, and at each increment recomputes the new set of $S$ parameters and the corresponding two-port gain. These parameters are large signal parameters.

As the variable elements are further altered, the computed two-port gain decreases, representing the saturation effect of the device. The point on the saturation characteristic that is sought is the point of maximum power-added efficiency, which corresponds to the point of maximum oscillator power output. This, for an FET, may be closely related to the device small signal gain, as done by Pucel, Bera, and Masse [13]. At this point of maximum oscillator power out, the computer prints out the large signal $S$ parameters. It is these $S$ parameters which are used for large signal oscillator or amplifier design. From these parameters, impedance values for amplifier conjugate match may be determined using well-known design equations for small signal amplifiers when maximum gain is desired [14], or those developed by Kotzebue when maximum added power is desired [15]. Impedance embedding elements may also be computed for six oscillator configurations using the equations developed by Kotzebue and Parrish [3].

Less complicated than the previous approach, and consequently less accurate, is the second design approach which may be preferred since the somewhat lengthy computer program required for the first approach, and the necessary information for providing the starting point circuit element values to the computer, may not be available.

In the second approach, advantage is taken of the fact that under large signals, the magnitude of $S_{21}$ varies much more than any other $S$ parameter, a fact verified by large signal measurements. The simplified design approach assumes, then, that all of the $S$ parameters except the magnitude of $S_{21}$ are constant under large signals. The large signal magnitude of $S_{21}$ is reduced, as before, to that value which corresponds to the maximum oscillator output power. The results obtained using this approach compare favorably with those obtained using the more complicated approach, at least for the transistors used in this study.

This summarizes the design approaches. It is, of course, necessary in the first approach to accurately measure large signal characteristics at some time, and to determine the relationship between variable parameters for the FET device. It is probably not necessary, however, to compute new relationships for each FET, since it is unlikely that the important variable parameters would be different for each device unless there had been significant process differences between device types.

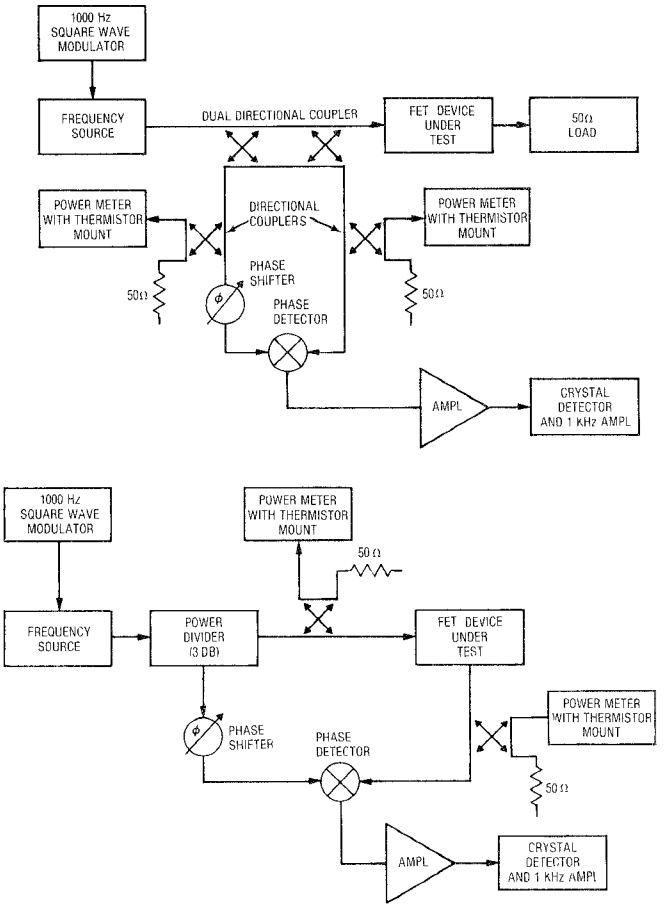



Fig. 2. $S$-parameter measurement test setup.

### B. Device Measurements

The device chosen for this study is an $X$-band GaAs MESFET which, when operated as an amplifier, is rated at 250-mW output at 10 GHz. The device is a one-cell geometry essentially the same as that described by Macksey *et al.* [15]. It has a gate width of 600 $\mu$m, with a gate length of about 1.2 $\mu$m. The device is packaged in the minicoax package in which the source is bonded to the ring of the package; the gate is bonded to the stud, and the drain is connected to the lid. This package is particularly well suited to oscillator application.

Small signal measurements of the FET were made first, to provide inputs to the computer program. The measurements were made using the Hewlett–Packard 8410 network analyzer system. The device was mounted on a coaxial test fixture with a thin metal ring making contact with the ring of the package for a grounded source configuration. The results for small signal measurements, from 8 to 12 GHz, are shown in Fig. 1. Also shown are the computed $S$ parameters for the device, which will be described later.

Large signal $S$ parameters were also measured, but because the network analyzer could not operate with power levels up to 400 mW, measurements were made using the setup shown in Fig. 2. Since this is a fairly standard technique, it will not be described in detail. Here the magnitudes of $S_{12}$ and $S_{21}$ were measured, as shown in Fig. 2(b), by measuring the power loss or gain through the device using calibrated directional couplers. For phase measurements, a phase shifter was placed in the line, and the input and output waves were summed in a mixer. The phase shifter was adjusted to give a minimum signal from the mixer corresponding to 180° phase cancellation. When the device was inserted, the phase difference was measured using a calibrated precision phase shifter. The difference in phase is the phase of $S_{12}$ or $S_{21}$, depending on which direction the device is inserted. $S_{11}$ and $S_{22}$ were measured similarly using the setup of Fig. 2(a) or the standard slotted line technique.

The results for the large signal $S$-parameter measurements at 10 GHz are shown in Fig. 3, in which the incident power is varied from 100 to 400 mW. Bias voltages were held constant in these measurements. If there were no changes in the $S$ parameters when the power level was increased, and if there were no changes in dc current due to rectification, the signal level was considered small. Small signal levels were below 100 mW for both input and output.

The question may be raised as to how meaningful these measurements are, since the voltage levels on input and output will differ from those in the measurements. A number of observations may be made in answer to this,

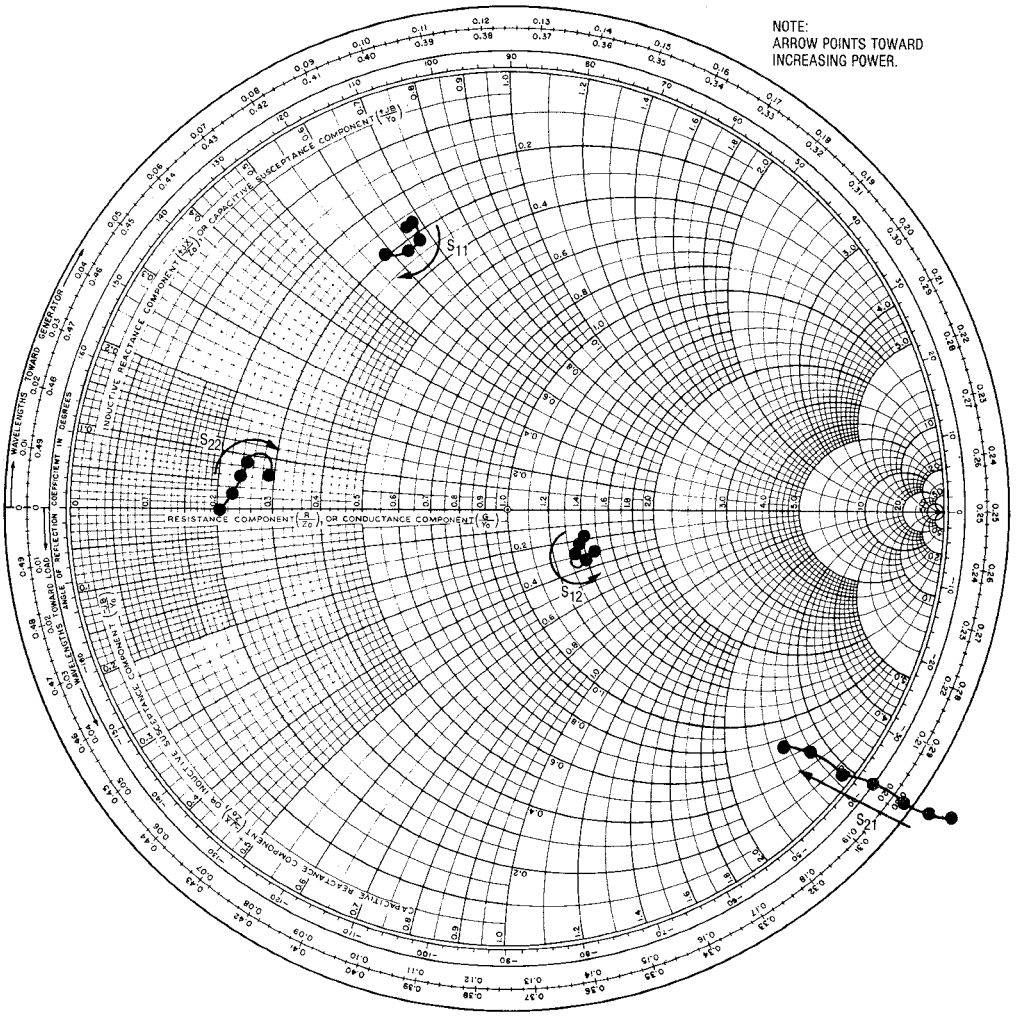



Fig. 3. GaAs FET large signal $S$-parameter measurements at 10 GHz.

which apply at least to the FET. First, as pointed out before, some meaningful design information was obtained even on the basis of small signal measurements. In particular, Maeda found that small signal measurements were adequate to predict frequency. This suggests that large signal effects produce primarily resistive changes. Second, Fig. 3 shows that the magnitude of $S_{21}$ changes with power much more than do the other parameters. Since $S_{21}$ is strongly influenced by the device transconductance $g_m$, it may be inferred that the changes in $g_m$ under large signals are a predominant factor. In that case, if the relative changes in the other parameters are somewhat in error due to differing voltages on input and output, the final effect would be relatively small. Finally, since the magnitude of $S$-parameter changes were measured to power levels greater than those corresponding to maximum oscillation power, the $S$-parameter changes for an oscillator would not reach the maximum changes shown in Fig. 3. Maximum oscillation power was 100 mW while the measurements were made, with up to 400 mW incident on the device. It was concluded, then, that even though there is some error in the large signal $S$-parameter measurements, it should not appreciably affect the computation of oscillator and amplifier embedding elements.

At this point, it will be shown how large signal measurements were used to predict the changes in equivalent circuit parameters under large signal conditions. Then, the series of mathematical relationships showing the large signal changes in the circuit parameters will be described for the FET studied. First, the device equivalent circuit will be considered.

### C. Device Equivalent Circuit

The equivalent circuit used for the FET chip was that suggested by Vendelin and Omori [16]. This equivalent circuit is shown in Fig. 4 in the dotted portion, excluding bonding inductances. Outside of the dotted portion, the package parasitic elements and circuit coupling elements are given. The inductances $L_G$, $L_D$, and $L_S$ represent the bonding wire inductances. In the minicoax package, with the FET chip located on the gate stud, $L_G$ would be quite small, representing only the post inductance inside the package. The capacitances $G_{GS}$, $C_{DS}$, and $C_{GD}$ represent the package parasitic capacitance plus some coupling

capacitance to the coax line. In the common source minicoax package, $C_{GD}$ would be extremely small, representing the capacitance inside the package between the gate stud and drain stud. Finally, $L_{GC}$, $L_{SC}$, and $L_{DC}$ are the coupling inductances to the coax line. To get some idea of the magnitude of these parasitics, the measurements by Monroe [17] of diode packages were used. The parasitics of the minicoax package were estimated from his measurements to provide initial values for the computer program. Initial values for other chip parameters were estimated from information supplied by the manufacturer, and from data in the paper by Vendelin and Omori [12].

In the equivalent circuit of Fig. 4, none of the parasitic parameters will vary under large signal conditions. Of the chip parameters, only the transit time $\tau_0$ would be constant under large signals since it is a function of device geometry. By the same token, it might be expected that the contact resistances would not be affected by large signals. However, when the FET begins to saturate, energy is converted to harmonic frequencies. This energy is dissipated in device and load resistances and, to a first approximation, appears to the equivalent circuit as if the resistive losses increased. Hence, they were included as, at least, potential variables under large signals.

### D. Computer Optimization Program

A computer program was written which takes equivalent circuit initial parameter values and computes a new set of $S$ parameters $S_{cij}$. These are compared with the inputted set of measured $S$ parameters $S_{Mij}$, and an error function generated as done by Vendelin and Omori [12]:

$$\text{E.F.} = \sum_{F=F_1}^{F_N} \{ W_1|S_{M11} - S_{c11}|^2 + W_2|S_{M12} - S_{c12}|^2 + W_3|S_{M21} - S_{c21}|^2 + W_4|S_{M22} - S_{c22}|^2 \} \quad (1)$$

where $F_1$ is the initial frequency, $F_N$ is the final frequency, and $W_i$ represents the weighting given to each set of $S$ parameters. Measured $S$ parameters for each frequency are stored in a file. The computed parameters are also stored, but continually change as the computed values get closer to the measured values.

In the optimization routine, selected parameters are varied randomly using a random number generator. The $S$ parameters and error function are computed, and the error is compared with the initial error. If the error is greater than the previous error computed, the parameters again are varied until a smaller error is computed. The "initial" circuit parameters are then reinitialized to the new value, and the parameters are again randomly varied. This procedure continues until some specified maximum number of comparisons is made, or until some maximum error is reached. The program then outputs the computed $S$ parameters and circuit element values.

A table of computed equivalent circuit values is given in column 1 of Table I for the FET used in this study. The next step taken was to input the measured large signal $S$ parameters at a couple of power levels, while holding constant the parasitic elements and $\tau_0$. This meant that seven parameters were varied. It was found that $R_F$, $C_F$, and $C_I$ could also be held constant with little increase in the error. The equivalent circuit values, which were computed for +24- and +26-dBm power levels, are shown in columns 2 and 3 of Table I. From these values, a tentative relationship between the relative changes in parameters was established.

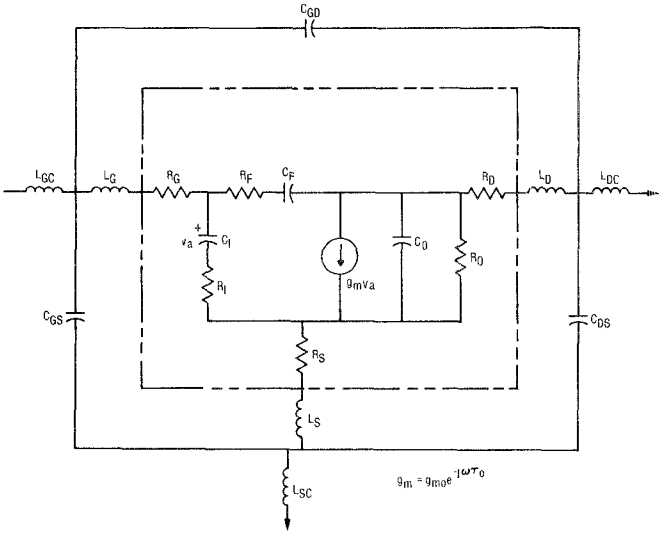



Fig. 4. FET equivalent circuit including package and mounting parasitics.

The only parameter which caused difficulty was $R_0$. The reason for this is apparent in Fig. 3 where it may be seen that at power levels greater than +24 dBm, $S_{22}$ abruptly changes. Below this point the changes are approximately linear with increasing power in dBm, as they are with $S_{21}$. Gain calculations based on $S$ parameters measured at +26 dBm show that the gain would be only 0.87 dB. Hence, the +26-dBm level is too far into saturation. With this limitation in accuracy, approximate proportional relationships between the parameters were found to be the following:

$$R_I \propto g_m^{-1.3}$$
$$R_0 \propto g_m^{0.7}$$
$$C_0 \propto g_m^{-0.7}. \quad (2)$$

In order to compute the large signal parameters at maximum oscillation power, the small signal equivalent circuit parameters were established by the computer optimization program as described. Then, the $g_m$ was decreased incrementally, with the other parameters varied in accordance with the relationships of (2). At each incremental reduction in $g_m$, the $S$ parameters were recomputed along with the gain. If one were interested in the 1-dB compression point, the $S$ parameters used would be those at that point. For oscillation or large signal amplifier

TABLE I
FET COMPUTED SMALL AND LARGE SIGNAL EQUIVALENT CIRCUIT PARAMETER VALUES

| FET EQUIVALENT CIRCUIT | (1) SMALL SIGNAL | (2) +26 dBm | (3) +24 dBm | (4) +24 dBm |
|---|---|---|---|---|
| LS = Source Parasitic Inductance(H)= | 0.200E-09 | | | |
| LD = Parasitic Inductance(H)= | 0.720E-09 | | | |
| LG = Gate Parasitic Inductance(H) | 0.133E-09 | | | |
| CGS = Gate to Source Parasitic Cap(F)= | 0.374E-12 | | | |
| CGD = Gate to Drain Parasitic Cap(F)= | 0.000E 00 | | | |
| CDS = Drain to Source Parasitic Cap(F)= | 0.321E-12 | | | |
| RI = Gate to Source in Res.(Ohms)= | 0.444E 01 | 7.31 | 6.28 | 6.33 |
| CI = Input Capacitance(Farads)= | 0.104E-11 | 0.928E-12 | 1.06E-11 | |
| CF = Feedback Capacitance(Farads)= | 0.416E-13 | 0.57E-13 | 0.728E-13 | |
| RO = Output Resistance(Ohms)= | 0.602E 03 | 296. | 394. | 491. |
| CO = Output Capacitance(Farads)= | 0.420E-13 | 0.608E-13 | 0.581E-13 | 0.483E-13 |
| RF = Feedback Resistance(Ohms)= | 0.207E 03 | 438. | 399. | |
| GMO = Low Freq Transconductance(Mhos)= | 0.235E-01 | 0.0152 | 0.0193 | 0.0181 |
| TO = Delay Time (Sec)= | 0.741E-11 | | | |
| LCS = Source Coupling Inductance(H)= | 0.000E 00 | | | |
| LCD = Drain Coupling Inductance(H)= | 0.624E-09 | | | |
| LCG = Gate Coupling Inductance(H)= | 0.415E-09 | | | |
| RS = Source Resistance(Ohms)= | 0.164E 01 | | | |
| RD = Drain Resistance(Ohms)= | 0.523E 00 | | | |
| RG = Gate Resistance(Ohms)= | 0.825E 00 | | | |

application, the point of maximum power added gain is of interest. This corresponds to the point of maximum oscillator power, which will now be determined.

### E. Maximum Oscillator Power

Pucel *et al.* [13] point out that the power-gain saturation characteristic of a FET power amplifier may be approximated by an equation of the form

$$P_0 \simeq \frac{G_0 P_{IN}}{1 + G_0 P_{IN}/P_{sat}} \tag{3}$$

where $G_0$ is the small signal gain and $P_{sat}$ is the saturated output power as an amplifier. The amplifier is tuned for *maximum efficient gain* $G_{ME}$ at each input power level. Maximum efficient gain is defined by Kotzebue as the power gain which maximizes the two-port added power, i.e., where

$$\frac{P_{out} - P_{IN}}{P_{IN}} = \text{maximum.} \tag{4}$$

In terms of $S$ parameters, this is given as

$$G_{ME} = \frac{\left|\frac{S_{21}}{S_{12}}\right|^2 - 1}{2\left\{K\left|\frac{S_{21}}{S_{12}}\right| - 1\right\}} \tag{5}$$

$$K = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{6}$$

where $K$ is the Rollett stability factor. Then, the input and output reflection coefficients $\Gamma_{IN}$ and $\Gamma_{OUT}$, respectively, are

$$\Gamma_{IN} = \left[S_{11} + \frac{S_{21}S_{12}\Gamma_{out}}{1 - S_{22}\Gamma_{out}}\right]^* \tag{7}$$

$$\Gamma_{OUT} = \left[S_{22} - \frac{S_{12}S_{21}}{1 + S_{11}}\right]^*. \tag{8}$$

The use of $G_{ME}$ is particularly well suited to large signal amplifier design.

A typical amplifier power saturation characteristic for a 1-W device is shown in Fig. 5. The maximum oscillator power occurs at the point of maximum $(P_{out} - P_{in})$, or where $\partial P_{out}/\partial P_{in} = 1$. A better approximation to this curve than given by (3) is the exponential form

$$P_{out} \simeq P_{sat}\left[1 - \exp\left(\frac{-G_0 P_{IN}}{P_{sat}}\right)\right]. \tag{9}$$

From this, the point of maximum oscillator power may be computed:

$$P_{OSC}(\max) = P_{sat}\left[1 - \frac{1}{G_0} - \frac{\ln G_0}{G_0}\right] \tag{10}$$

and the maximum efficient gain $G_{ME}$, therefore, is

$$G_{ME}(\text{max oscillator power}) = \frac{G_0 - 1}{\ln G_0}. \tag{11}$$

Thus for example, an FET having a small signal $G_{ME} = 7.5$ dB with a saturated amplifier output power of 1 W would be capable of a maximum oscillator power of 515 mW. The maximum gain at this point is 4.3 dB.

The gain expression of (11) was used to determine at what gain level the large signal $S$ parameters were to be

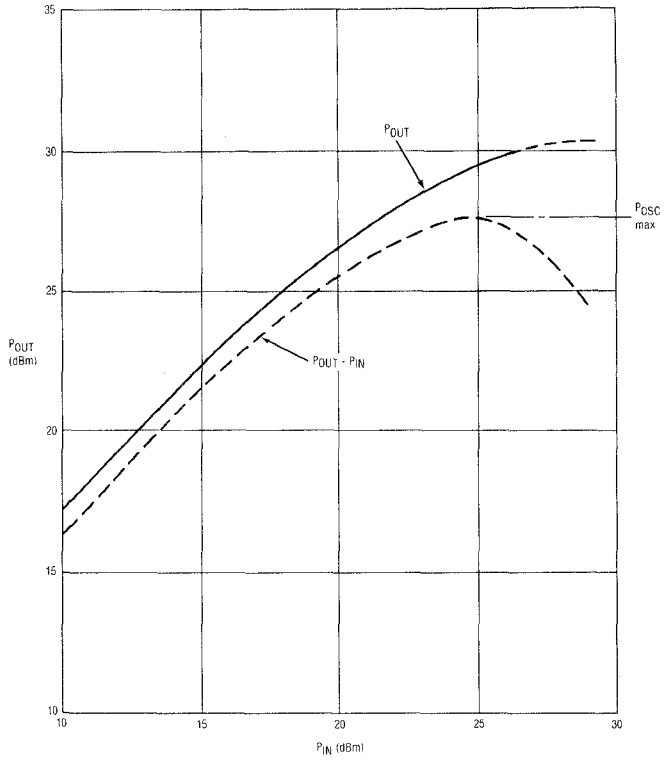



Fig. 5. Gain saturation characteristic on a 1-W FET power amplifier.

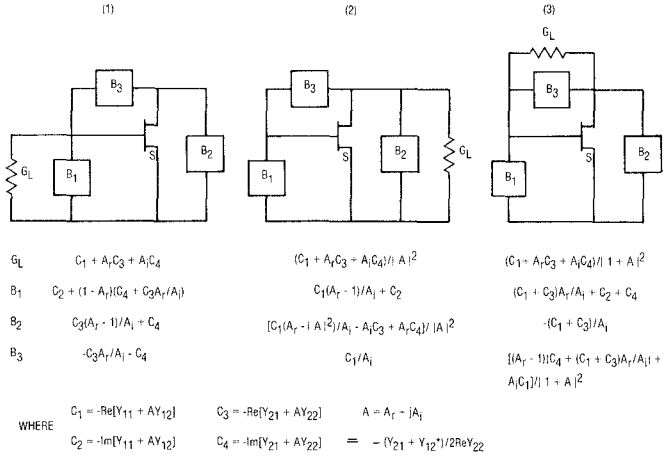


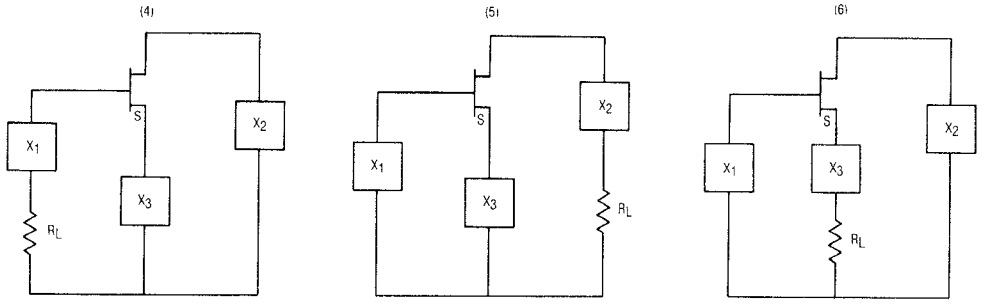

Fig. 6. Optimum embedded elements for three shunt oscillators (from Kotzebue and Parrish [3]).

used for oscillator application. Notice that it is not necessary to know the saturated output power of the transistor. All that is needed is a measurement of $S$ parameters at a number of frequencies. Normally, these are available from the transistor manufacturer.

### *F. Oscillator Circuit Design*

Having computed the large signal $S$ parameters following the procedure outlined before, the embedding elements for six oscillator topologies may be computed [3]. Three shunt oscillator configurations with the design equations for the optimum embedding elements are given in Fig. 6, and three series oscillator configurations are given in Fig. 7. Design equations are given in terms of $Y$ and $Z$ parameters in the figures which may be readily transformed to $S$ parameters by the usual $S$ to $Y$ and $Z$ conversion formulas. It may be added that there are, of course, other possible configurations consisting of series and shunt element combinations, but of these six, generally one or more will result in a practical design.

For the transistor which was measured, the six oscillator circuits embedding element values are given in Fig. 8. Not all of these circuit configurations can be readily realized in practice. In particular, all of the shunt oscillator config-




| | (4) | (5) | (6) |
|---|---|---|---|
| $R_L$ | $D_1 + F_rD_3 + F_iD_4$ | $(D_1 + F_rD_3 - F_iD_4)/\lvert F\rvert^2$ | $(D_1 + F_rD_3 - F_iD_4)/\lvert 1 - F\rvert^2$ |
| $X_1$ | $D_2 - (1 + F_r)(D_4 + D_3F_r/F_i)$ | $D_1(1 + F_r)/F_i + D_2$ | $(D_1 - D_3)F_r/F_i + D_2 - D_4$ |
| $X_2$ | $-D_3(1 + F_r)/F_i - D_4$ | $[D_1(F_r + \lvert F\rvert^2)/F_i - F_iD_3 - F_rD_4]/\lvert F\rvert^2$ | $(D_1 - D_3)/F_i$ |
| $X_3$ | $D_3F_r/F_i + D_4$ | $-D_1/F_i$ | $[(1 + F_r)D_4 - (D_1 - D_3)F_r/F_i - F_iD_1]/\lvert 1 + F\rvert^2$ |

WHERE

$D_1 = -\mathrm{Re}[Z_{11} + F Z_{12}]$ $\quad D_3 = -\mathrm{Re}[Z_{21} + F Z_{22}]$ $\quad F = F_r - jF_i$

$D_2 = -\mathrm{Im}[Z_{11} + F Z_{12}]$ $\quad D_4 = -\mathrm{Im}[Z_{21} + F Z_{22}]$ $\quad = (Z_{21} - AZ_{11})/AZ_{12} - Z_{22})$

Fig. 7. Optimum embedding elements for three series oscillators (from Kotzebue and Parrish [3]).

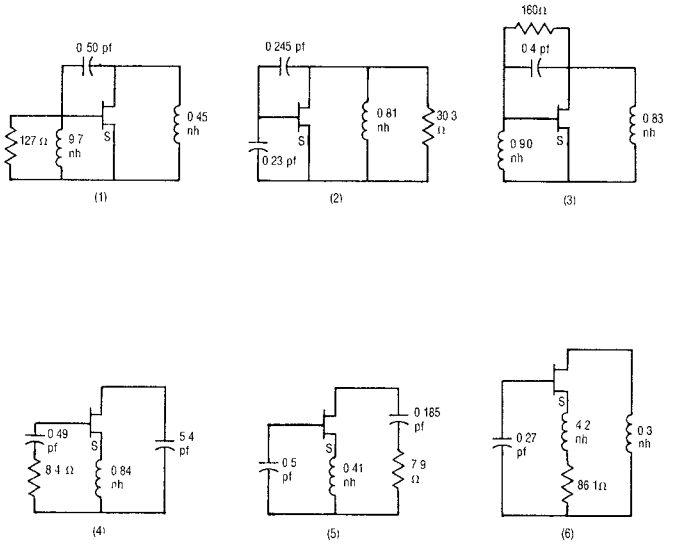



Fig. 8. Computed values of embedding elements for FET oscillator, MSX801G FET device. (a) Values for three shunt oscillators. (b) Values for three series oscillators.

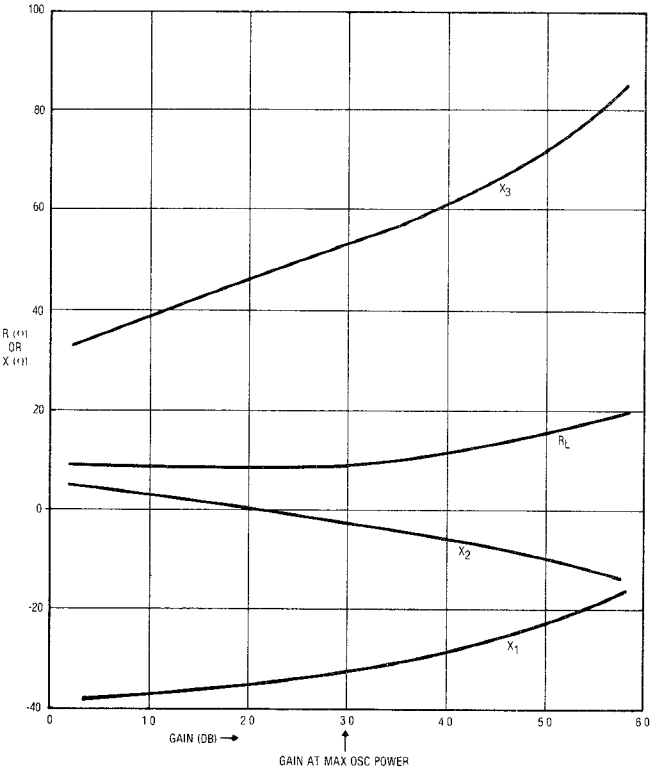



Fig. 9. Plot of computed optimum oscillator embedding elements as a function of two-port gain for circuit 4 at 10 GHz.

urations are difficult to realize with a coax packaged device. This is due to the fact that there is no easy way physically to locate a capacitor between the gate and drain since the source ring gets in the way. The series circuits are more amenable to fabrication, particularly circuit 4 of Fig. 8. Since it is of interest to know how critical the embedding element values are as a function of signal level, Fig. 9 gives a plot of these element values as a function of two-port maximum efficient gain. Small signal levels correspond to a gain of 5.7 dB while the gain at maximum oscillator power is 3.0 dB. The figure shows that there is a significant change in oscillator embedding element values for small and large signal conditions. Likewise, Fig. 10 is a plot of embedding element values as a function of frequency for circuit 4. Again, it may be seen that the values do vary considerably with frequency.

### G. Experimental Results

The oscillator which was designed and built to verify the theory was the series configuration, circuit 4 of Fig. 8. A coaxial realization of this circuit is shown in Fig. 11. The inductance from the source lead was provided by a

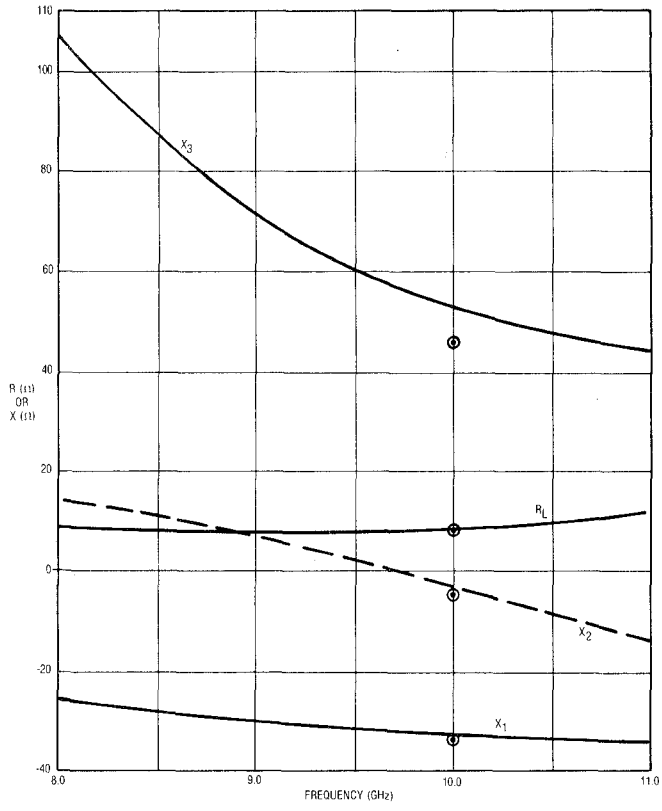



Fig. 10. Plot of optimum oscillator embedding elements as a function of frequency for circuit 4 at optimum power out.

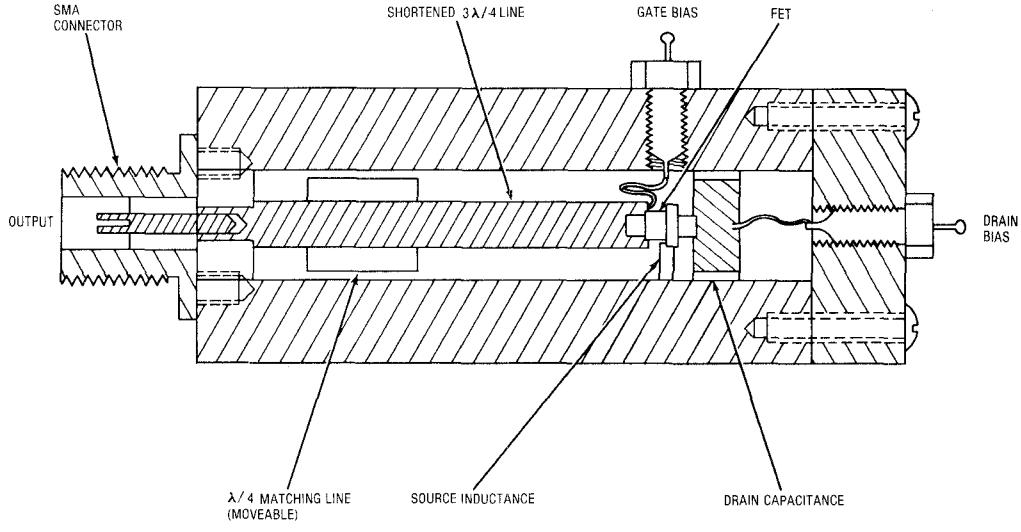



Fig. 11. Coaxial circuit FET oscillator. Realization of series oscillator configuration (4).

short length of line to the outer conductor wall of the oscillator cavity. Unfortunately, the exact size of this line was difficult to compute due to stray reactances in the shunt mounting of the short rod. The capacitance in series with the drain was obtained by use of a short length of low impedance line as shown. The series capacitance and load inductance were obtained by transforming down a shortened $\lambda/2$ 50-Ω line to a point of zero reactance, and using a $\lambda/4$ transformer to provide the correct series resistive loading at the FET of 8.9 Ω. In this circuit, the quarter-wave transformer was made movable to test the tunability of this circuit. The $\lambda/2$ line was used to increase the unloaded $Q$ of the circuit. Since the source was grounded to the wall of the cavity, it was necessary to use a dc block on the output which is not shown in Fig. 11. Anticipated output power was $P_0 = 0.38 P_{sat}$ and, since

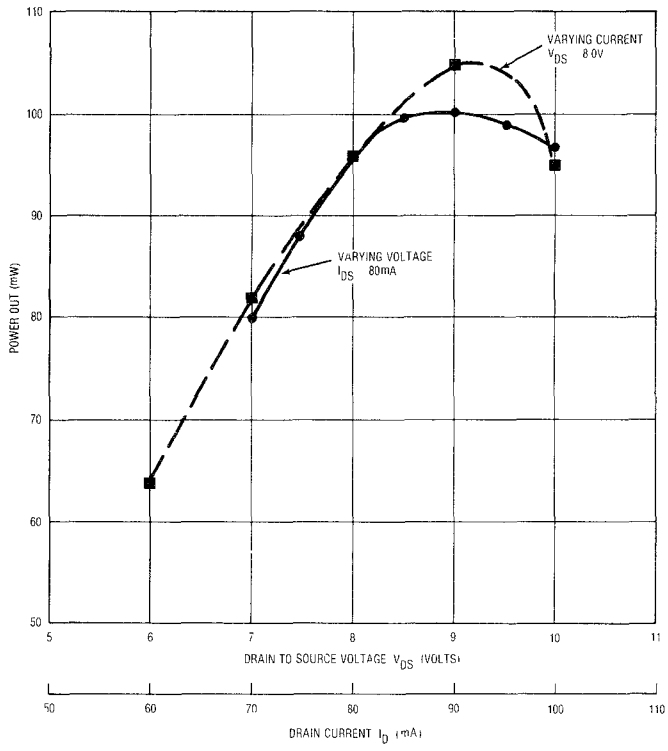



Fig. 12. FET oscillator power out versus drain-to-source voltage and drain current.

the device had a saturated output power of 250 mW at 10 GHz, then $P_0$ should be 95 mW. Measured output power at 10 GHz was 100 mW as computed. Fig. 12 is a plot of the measured oscillator power as a function of dc drain-to-source voltage $V_{ds}$ and drain current $I_d$. Notice that a dc-to-RF efficiency of 15 percent was obtained at 8 V and 90 mA at 10 GHz.

Although no special tuning was necessary to obtain maximum output power, it was found that with the load coupled as designed to give maximum output power, the oscillator tended to be susceptible to either not oscillating at all, or oscillating at full power. This indicated that the negative resistance was so close to its maximum value that, with a slightly larger load resistance, the net zero resistance condition for oscillations was not met. It was concluded that a slightly smaller load resistance should be used to assure oscillations at the desired frequency, even though the output power might be slightly less than the maximum available.

Since the oscillator tended to not oscillate under some temperature conditions, it was retuned to 9.5 GHz in order to make temperature measurements. The oscillator frequency increased 65 MHz when reduced to −40 from +25°C and its power increased to 125 mW. When increasing the temperature from +25 to +70°C, the frequency decreased 20 MHz while the power fell to 28 mW. By increasing the drain current to 90 mA, the power came up to 60 mW. This means that, for optimum oscillator design, $S$ parameters should be measured at the maximum temperature of operation to assure good performance.

## III. Second Design Approach

Up to this point, the design has been based entirely on the first approach, using computer optimization, to calculate large signal $S$ parameters. In the second approach, just the magnitude of $S_{21}$ is reduced until the point of maximum oscillator power is achieved. To see how close the oscillator embedding elements would be to the values obtained for the first approach, measured small-signal parameters at 10 GHz were used to compute these values, except for $S_{21}$ which was reduced in magnitude to a value of 0.735. This corresponds to $G_{ME}=2.96$, the value that would be calculated from (11). The value of small signal gain $G_0$ is calculated from (5) using the small signal magnitude of $S_{21}=1.03$.

Results of oscillator embedding element calculations at 10 GHz are shown as circled points in Fig. 10 for circuit 4. The differences are very small; hence, it is expected that oscillator design based on this method would be quite close to the first approach. This depends to some extent on how accurately the $S$ parameters are measured.

## IV. Conclusion

Techniques have been described which permit accurate FET oscillator design without repeated large signal measurements. Using these techniques, a coaxial cavity FET oscillator was constructed which substantially verified the theory.

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# IF Conversion Gain of Glow Discharge Lamps as *X*-Band Mixers for High LO Power Levels

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*Abstract*—**Inexpensive glow discharge indicator lamps mounted in a waveguide mount are investigated as mixers at relatively high *X*-band local oscillator (LO) power levels. The IF conversion efficiency was found to drop off for LO power levels greater than about 30–40 mW, although no damage occurs to the lamps at higher power levels. Because of the small lamp size relative to waveguide cross section, sensitivity is much less than in the free space configuration. For many reasons the use of such devices as mixers should be much more promising at millimeter-wave frequencies than at microwave frequencies.**

## I. Introduction

COMMERCIAL glow discharge indicator lamps, whose individual price is ordinarily a fraction of a dollar, have been shown to exhibit rather good sensitivity to both millimeter-wave [1], [2] and microwave [3]–[5] radiation as video detectors. Utilization of this type of device for detection of electromagnetic radiation has been extended to the infrared [6], [7], visible [8]–[13], and ultraviolet [14], [15] spectral regions. The ability to sense microwave frequency with such devices has also been demonstrated [16], [17]. Other advantages of gas discharges as detectors of electromagnetic radiation include less sensitivity to ambient temperature changes [18]–[20], large dynamic range and electronic ruggedness, wide-band RF response [1], [17]–[20], and the ability to detect sudden increases in radiation levels without being damaged [17], [19], [20]. Also, they can be used in environments such as the Van Allen belt, nuclear reactors, or space systems subject to intense ionizing radiation fields [21], [22] where many other types of detectors cannot operate reliably.

The chief disadvantage is a relatively slow response ($\approx$1-$\mu$s rise time). However, the rise time is limited, not by the intrinsic detection mechanism [17], [23], but by the parasitic reactance [9]. Recent experiments indicate that such reactance effects might be minimized and rise time thus improved by miniaturizing the electrode geometry [23]. The very high intrinsic speed of response by the gas discharge *itself* is clear from the many harmonic generation and wide-band frequency-mixing operations that have been observed at frequencies as high as the optical spectral region [24]–[28]. However, as in such experiments the output is an electromagnetic wave rather than an electronic voltage signal, reactance has no effect [23].

Recent experiments have indicated the feasibility of using simple inexpensive glow discharge indicator lamps as mixers at millimeter-wave [29] and microwave [30] frequencies. In particular, one suggested advantage of such an application, in addition to low price, is to exploit the wide dynamic range of these devices by illuminating them with relatively high local oscillator (LO) power levels $P_{LO}$ so as to make possible detection of very weak signal power levels $P_S$ [30]. This is possible in principle because the IF signal is proportional to $(P_S P_{LO})^{1/2}$. Thus as long as the product of $P_S$ and $P_{LO}$ does not vary much, high LO levels may in theory compensate for weak signal levels. That varying one IF component is equivalent to varying the other has been verified for low signal and LO components [30]. The purpose of this paper is to report sensitivity limitations observed at higher *X*-band power levels with inexpensive commercial indicator lamps in

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